Sx4000
SDR ASIC

SatixFy

Revolutionary On-Board Processing Space Grade Chip

DVB-S2X/RCS2 Software Defined Radio chip for regenerative on-board processing and transparent satellite systems, based on proven SatixFy SDR technology. Suitable for all space based missions and Satellite Gateway application.

REGENERATIVE / TRANSPARENT SDR MODEM SoC

KEY FEATURES

+ Future proof Software Defined Radio implementation
+ Transparent and Regenerative ASIC
+ Enable independent user, gateway and inter-satellite links
+ DVB-S2X/RCS2 compliance with Beam-Hopping support
+ Multi-channel receive/transmit with flexible bandwidth allocation (2GHz processed Bandwidth, up to 16 DVB-S2X/RCS2 carriers)
+ SerDes interface compliant with JESD 204B/C for ADC/DAC /FPGA connectivity
+ Embedded multi-Gbps data switching/routing for LEO constellations and ISL links
+ Radiation hardened, compatible with LEO/MEO/GEO orbits
+ Powerful Quad Core ARM53 CPU, two fast DSP for Telecom (>10,400 DMIPs)
+ Densest performances per Watt, per Kilo for Ground and Space applications
+ Linux drivers API support
+ Scalable architecture connecting multiple Sx4000 together to fit any size payload

APPLICATIONS:

+ Space: On-Board-Computer, Payload TT&C, Telecom and EO processors
+ Ground Applications: DVB-S2X/RCS2 Satellite Gateway, VSAT modems

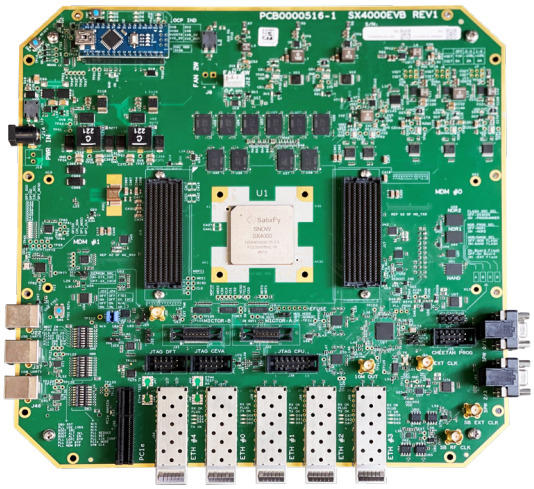
Sx4000

Evaluation Board & Software Development Package

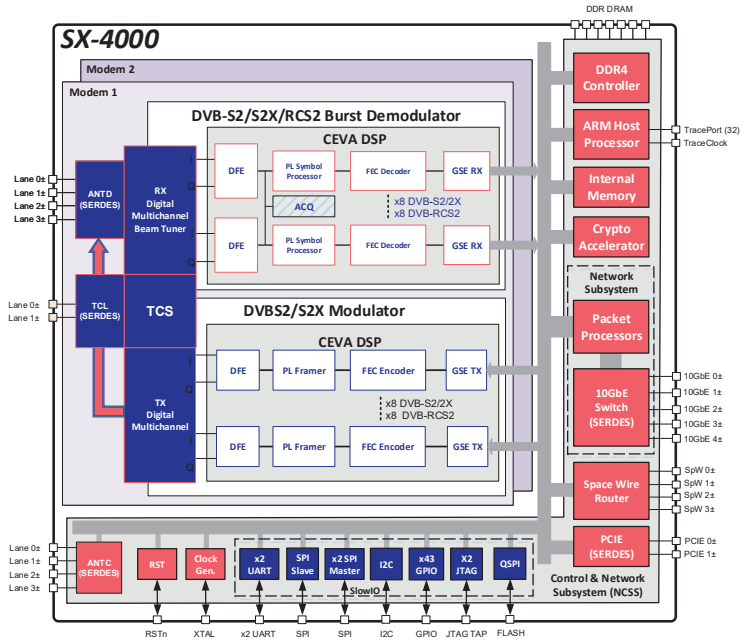
Sx4000 evaluation platform offersoptions to evaluate the ASIC performance as well demonstrate regenerative or transparent payload systems. SatixFy provides an Embedded Software Layer, including DSP code for all supported waveforms, DVB-S2X including super frame transmit and receive, DVB-RCS2, basic networking software, Linux drivers for all functions and complete Linux SDK. The EVB supports multiple Sx4000 EV board connections to rapidly demonstrate payload functionality requiring multiple GHz (>2GHz) processing. The EV board offers a seamless interface to SatixFy PRIME Digital BeamFormer Evaluation boards.

Evaluation Package
Provides complete infrastructure needed to test the chip's functionality and demonstrate its performance

Basic Software Development Package
Linux SDK, provides the ability to configure the ASIC and run standard payload application



HIGH-LEVEL ARCHITECTURE



TECHNICAL SPECIFICATIONS

Symbol rate	2 Gsymbol/s (2x 1 Gs/s)
VLSNR & ELSNR	>= -20dB
Regenerative	GSE processing and switching
Transparent	2GHz capacity, up to 16 channels
Data rate	10 Gbps
Roll-off	Programmable: 1% to 50% (1% or less granularity)
Beam Hopping	Superframe-based acquisition
	DVB-S2X-based acquisition
Modulation and Coding	**Modulations:**
	BPSK, QPSK, 8PSK, 16 APSK, 32 APSK, 64 APSK, 128 APSK, 256 APSK and VL SNR
	Code rates:
	According to S2 and S2X MODCOD definition | Frame length: 16200, 64800, 32400
System Expansion	5 port Ethernet switch (10 Gbps per port)
	4 Transparent Channel Lanes (TCL @25Gbps) expansion
Cryptography support	Secure boot
	On the fly data encryption/decryption
Digital Connectivity	JESD204C (25Gbps)
Target orbits	LEO, GEO, MEO, HEO
Radiation mitigation	TID: > 100krad(Si)
	SEL: < 60Mev*cm2/mg
	SEU rate < 10^{-8} events/bit-day
Operating life	15 – 18 years
CPU	Quad core ARM A53 @ 1GHz
DSP	4 x CEVA DSP @ 1Ghz

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